

Flexible Interconnect Design Using a Mechanically-Focused, Multi-Objective Genetic Algorithm

Joe L. Gonzalez[✉], Student Member, IEEE, Paul K. Jo[✉], Student Member, IEEE, Reza Abbaspour, Student Member, IEEE, and Muhannad S. Bakir, Senior Member, IEEE

Abstract—This paper presents a multi-objective optimization process using a non-dominated sorting genetic algorithm-II that aims to maximize the vertical displacement of MEMS-type mechanically flexible interconnects (MFIs) while simultaneously preventing these interconnects from experiencing plastic deformation. Given an initial MFI geometric body, this process seeks to optimize the photomask interconnect design so that no modification is required for the existing fabrication process flow. After the design optimization, a reflowed polymer-dome microfabrication process is employed to fabricate the NiW MFIs to provide a more complete analysis of this paper. Simulation data shows that the optimized design can achieve up to 29.7% greater vertical displacement before experiencing plastic deformation relative to the initial design. Experimental data shows an average of 34.2% less vertical plastic deformation relative to the initial design when the MFIs are indented to a depth of 45 μm . In both simulation and experimental scenarios, the optimized MFIs demonstrate less stress/plastic deformation relative to the initial MFIs for the same given indented depth. [2017-0229]

Index Terms—Flexible interconnects, 2.5D/3D integration, genetic algorithms, multi-objective optimization, NiW interconnects, interconnect design.

I. INTRODUCTION

Mechanical properties of MEMS-type flexible interconnects often provide advantages in various microelectronic applications for their ability to address certain packaging and assembly challenges normally associated with conventional die-to-package (including 2.5D) and 3D IC systems [1]–[20]. Specifically, properly designed flexible interconnects possess several advantages over solder bump interconnect technology, and these advantages are often mechanical in nature. One challenge of fine pitch solder-based microbumps is their bridging with one another during the thermocompression bonding process due to the lateral spreading of the melting solder, an issue that is likely to grow more prevalent as pitch scales down. Moreover, fine pitch solder-based microbumps, possessing a higher composition of

intermetallic compounds (IMCs) after bonding, are more brittle at the joint, hence compromising the mechanical integrity of the microbump interconnect [21], [22]. Additionally, for C4 bumps, underfill is often required owing to the coefficient of thermal expansion (CTE) mismatch between the package and die requiring interconnecting, especially since the advent of low-K flip-chip packaging [23]–[28]. Moreover, the higher dielectric constant of underfill relative to air can negatively impact signal integrity and/or contribute to unwanted cross-talk in high frequency or high-speed/high-edge-rate digital applications [29], [30].

With properly designed MEMS-type flexible interconnects in their place, no thermocompression bonding is required and hence no brittle and permanent metallurgical bonds are formed, no underfill is necessary which not only greatly simplifies the packaging process but contributes to better signal integrity, and since no phase change occurs in the interconnects during the assembly process, the issue of bridging is avoided. However, although flexible interconnects may avoid many of the pitfalls seen in solder bumps, this point does not imply that flexible interconnects have no potential issues of their own. For example, although no brittle metallurgical bonds are formed during the assembly process, this fact does not imply that these interconnects are not subject to fracture. Additionally, poorly designed flexible interconnects may require underfill if they cannot sufficiently mitigate warpage. The prevention of “white bump” failure on low-K die, the ability to pass certain drop or shock tests for mobile devices, and a certain minimum fatigue life to achieve desired system robustness and reliability are additional critical features that certain flexible interconnects must meet. Alternatively, obtaining such desired mechanical properties in flexible interconnects is not generally a trivial matter. Therefore, this paper introduces a design approach that aims to optimize the interconnect geometry such that these interconnects are properly tailored for the applications their targeted to serve. Figure 1 illustrates some of these applications.

Manuscript received September 17, 2017; revised April 27, 2018; accepted May 27, 2018. Date of publication June 20, 2018; date of current version July 31, 2018. This work was supported by the National Science Foundation under Grant ECCS-1542174. Subject Editor L. Spangler. (Corresponding author: Joe L. Gonzalez.)

The authors are with the Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: jgonzalez34@gatech.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JMEMS.2018.2843809

There exist a range of flexible interconnects for specialized applications [1]–[12], [15]–[20], [31]–[36] that are focused on fabrication technology development and not specifically on what design(s) may optimize their mechanical/electrical performance. Nevertheless, the potential to optimize these designs exists. Other optimization works in the field have developed

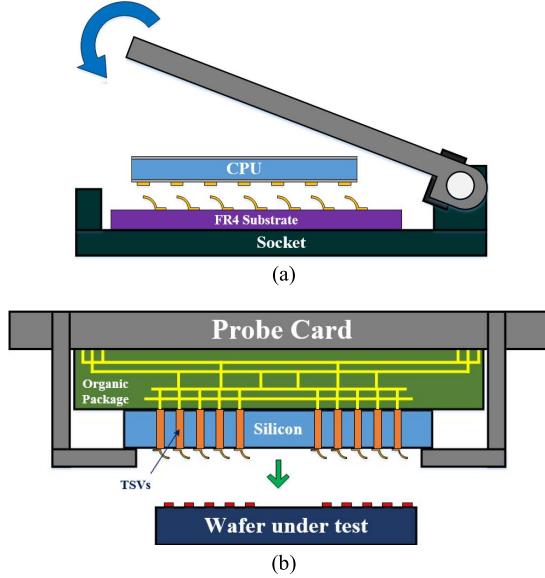


Fig. 1. Different flexible interconnect applications and uses including (a) LGA socket with flexible interconnects that allows for the placing and replacing of CPUs and other die and (b) wafer-level testing with flexible interconnects, which compensate for the non-planar surface of the wafer in addition to providing temporary connections that enable repeatable testing.

their own particular approach to optimizing the performance of flexible interconnects upon which we attempt to expand via attempting to further generalize the overall optimization process in addition to demonstrating experimental data for our optimized outcome [6], [37], [38]. The work presented in this paper focuses not only on the optimization process itself, but it also offers a simplified means to implement this process for a large range of MEMS-type flexible interconnect technologies, regardless of the specific fabrication process flow via: 1) optimizing only the photomask design of the interconnect and 2) implementing a spline-based parametrization in addition to more conventional parametrizations (e.g., widths, radii, etc.) of the interconnect geometry so that this optimization process is flexible enough to accommodate a large variety of geometric designs (that are to be optimized).

In this paper, we present: 1) an attempt at a generalized multi-objective optimization approach that is applicable to a wide variety of flexible interconnects, 2) the optimization of MEMS-type mechanically flexible interconnects (MFIs) as a proof-of-concept, 3) the extraction of certain structural properties of microfabricated MFIs from the measured data, and 4) a comparison between the optimized and initial MFI structures for both simulation and experimental scenarios.

II. DESIGN APPROACH

To demonstrate the workings of our multi-objective optimization process, we use as a proof-of-concept our prior work on MEMS-type MFIs [32]–[34]. The design targeted is the photomask design; this approach avoids modifying the fabrication process flow and hence simplifies efforts to improve the MFI's mechanical properties. Additionally, the targeting of the photomask design allows for extensive design freedom as virtually any shape can be achieved.

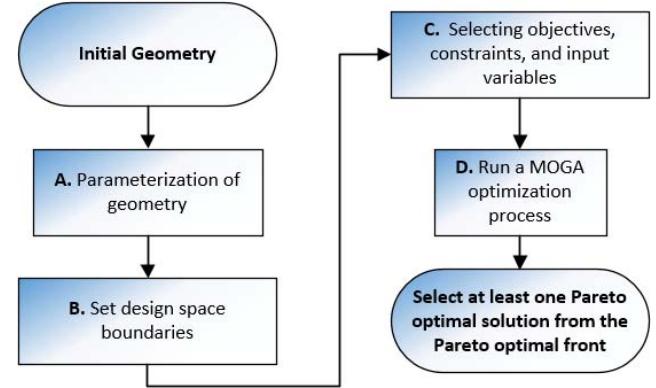


Fig. 2. Flowchart of the optimization methodology process.

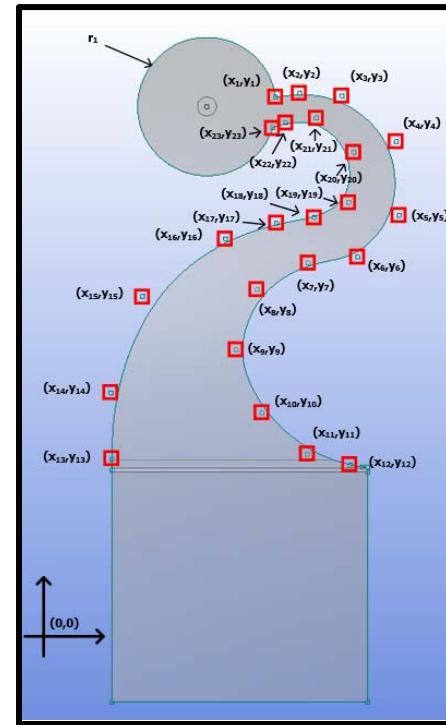


Fig. 3. Parametrization of the MFI as a collection of spline control point (x,y) coordinates. Additionally, the radius of the MFI "head/tip" is also a parameter.

Figure 2 illustrates a flowchart of the overall optimization methodology process presented here. We follow this design flow below.

A. Parametrization of Geometry

We first parametrize our initial design as mostly a collection of spline control points, as seen in Figure 3. These control points determine the shape of the overall spline, allowing for a very fluid exploration of different designs. Additionally, a spline-based geometry allows for a continuity in the curvature profile of the interconnect, hence it is more likely to avoid high stress corners relative to geometries comprised of an abrupt connection of curves, lines, etc. This continuity in the curvature profile also helps the mesh processing as stress

TABLE I
INPUT AND OBJECTIVE VARIABLES

Input Variables	Objective Variables
(x,y) coordinates of the 23 spline points	Maximum von Mises stress
MFI tip radius	Mechanical compliance
Vertical displacement	Vertical displacement

singularities are avoided along the spline. Therefore, via modifying the (x, y) coordinates of the spline control points, the shape of the MFI mask geometry is effectively modified. Additionally, in this case, the radius of the head or tip of the MFI is also a parameter that partially controls the photomask geometry.

B. Set Design Space Boundaries

After parametrizing the interconnect geometry, our optimization process calls to impose the design space boundaries. Specifically, each (x,y) coordinate of the MFI spline control points and the radius of the MFI tip must fall within some specified ranges. These ranges must be chosen so to avoid any intersecting and hence non-physical geometries and also to constrain the interconnect geometry from becoming too large.

C. Selecting Objectives, Constraints, and Input Variables

After setting the design space boundaries, the objectives, constraints, and input variables of the multi-objective genetic algorithm are selected. Table I shows the input and objective variables used in this paper. Note that in this case, vertical displacement acts as both an input and objective variable (discussed in Section III).

For demonstration purposes, the improved mechanical robustness of the interconnect is the targeted outcome. More specifically, we are targeting the improvement of the mechanical robustness of the interconnect in scenarios where the interconnect is utilized as a temporary probing mechanism (e.g., probe cards, etc.).

To obtain the aforementioned outcome, the objective variables that we seek to optimize include: 1) the maximum von Mises stress within the interconnect, 2) the vertical (z-axis) displacement imposed upon the tip of the MFI, and 3) the mechanical compliance of the MFI. In short, our optimization process seeks to minimize the aforementioned maximum von Mises stress while simultaneously maximizing the vertical displacement of the MFI. Additionally, we impose a constraint upon the compliance of the MFI to stay within a specified range of 2 mm/N to 10 mm/N. In this specific demonstration, the reason for an upper limit on compliance is due to contact resistance considerations.

No surrogate model was used but instead a direct approach was pursued to achieve a more accurate optimization process. However, to expedite the process, a surrogate model such as Kriging (useful for computer experiments such as FEA-based simulations) may prove useful [39].

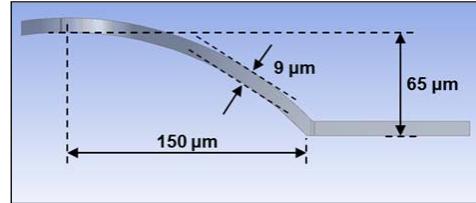


Fig. 4. MFI side-geometry and corresponding dimensions.

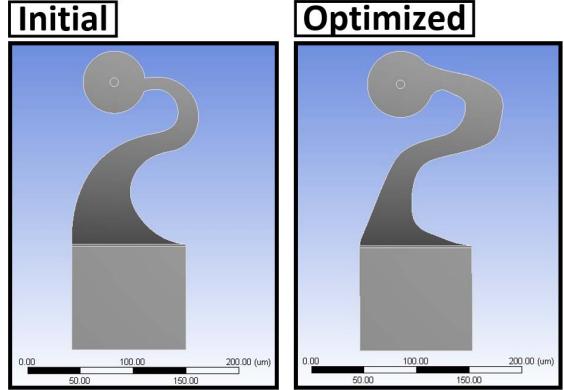


Fig. 5. Geometry comparison of the initial, non-optimized MFI (left) and optimized MFI (right).

D. MOGA Optimization Process

After performing an optimal space-filling design of experiment (DOE), a multi-objective non-dominated sorting genetic algorithm-II (NSGA-II) is implemented. The optimization process eventually converges once the change in the mean and the standard deviation of max von Mises stress values and vertical displacement values are 2% or less relative to these same values in the previous generation.

III. FEA-BASED OPTIMIZED RESULTS AND DISCUSSION

A. FEA-Based Results and Discussions

As seen in Figure 4, the initial MFI design has a stand-off height of 65 μm , a length of 150 μm from its anchor junction to the peak of the MFI tip, and a thickness of 9 μm . These dimensions are purposely left unchanged during the optimization process to minimize any modifications to the fabrication process. Modifying the photomask design, alternatively, is straightforward.

Figure 5 shows this optimized MFI (on the right) alongside the initial, non-optimized MFI (on the left). As is seen, the optimized MFI clearly has a different geometry relative to the initial MFI design.

ANSYS Workbench is used to evaluate the max von Mises stress in the MFIs. Furthermore, a nickel tungsten (NiW) alloy is chosen as the material of the MFI due to the relatively high yield strength that it can achieve (1.93 GPa [40]) compared to copper (Cu). This 1.93 GPa yield strength for NiW is used in the simulations. The NiW Young's modulus used was 180 GPa [40]. Using ANSYS Workbench, both MFIs (initial and optimized) are indented vertically (z-axis) at their tips to a depth of 24 μm , which results in only elastic deformation

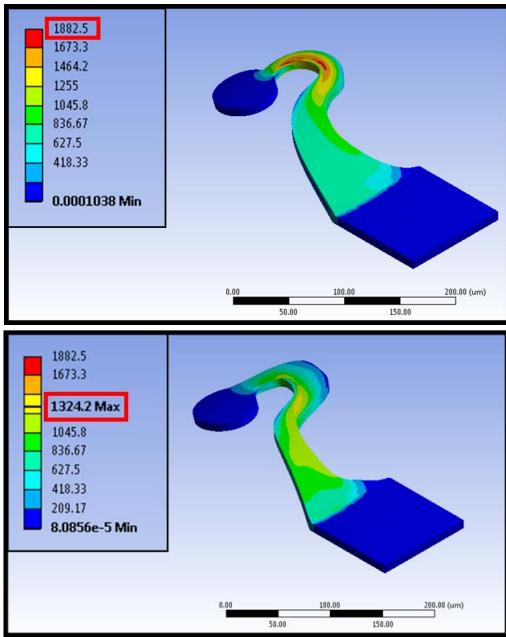


Fig. 6. Von Mises stress results (in MPa) of the initial and optimized MFIs. A 29.7% decrease in max stress (1.88 GPa \rightarrow 1.32 GPa at 24 μm) is observed in the optimized MFI relative to the initial MFI.

TABLE II
OPTIMIZATION RESULTS

	Max von Mises Stress (MPa)	Compliance (mm/N)
Initial MFI	1882.5	4.93
Optimized MFI	1324.2	5.52

in both MFIs (max. von Mises stress is below the NiW yield strength). The results are shown in Figure 6 and in Table II. As is seen, for a 24 μm vertical displacement, the maximum von Mises stresses in the initial MFI and in the optimized MFI are 1882.5 MPa and 1324.2 MPa, respectively. Furthermore, the compliances of the initial MFI and the optimized MFI are 4.93 mm/N and 5.52 mm/N, respectively. Therefore, the optimization process resulted in a design that lowered max stress by 29.7% relative to the initial design while achieving a compliance of 5.52 mm/N within the targeted range of 2 mm/N to 10 mm/N.

Since simulations involving plastic deformation are more complex and hence slower, plastic deformations were ignored in the optimization process for simplicity and instead, all behavior was considered elastic. The omission of plastic deformation was also beneficial for the optimization process itself.

Specifically, when the yield strength of a material is exceeded, the stress/strain ratio decreases and hence any additional strain is associated with a lesser increase in stress relative to increases in strain that occur within the elastic region. From the perspective of the optimization process, this change in stress/strain ratio between the elastic region and the plastic region creates a scenario where increases in strain in the elastic region are penalized more heavily (i.e., higher relative

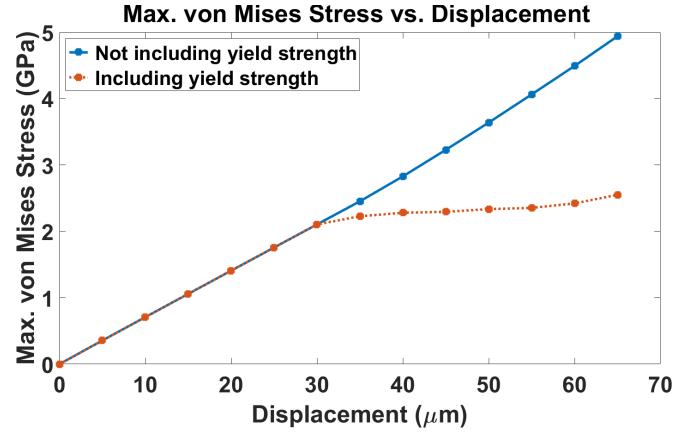


Fig. 7. Maximum von Mises stress vs. displacement, with and without the incorporation of a plastic deformation model. If yield strength is considered, max. stresses that exceed the yield strength of 1.93 GPa used in the simulations do not increase as quickly as stresses lower than yield strength. In an optimization framework, these “above yield strength” stresses are penalized on a different scale than stresses below yield strength, which is not the intent of the optimization process.

stress) than increases in strain in the plastic region, which is not the intent of the optimization process. This concept is illustrated in Figure 7.

Figure 8 demonstrates several Pareto fronts of the Pareto-optimal solutions from the multi-objective NSGA-II optimization process. As observed in this figure, the solutions begin to converge near the left side of the graph until they finally converge at the final Pareto front (most left). Since all the solutions at the final front are Pareto optimal, it is left up to the designer’s discretion to choose among these solutions. However, in this specific case, since one of the output variables is vertical displacement, it is possible that these “different” solutions result in the same MFI design. Therefore, to choose the final optimized solution, all the Pareto-optimal solutions were vertically indented at the same depth (this depth may be application specific). From these solutions, the selected MFI design exhibits the least amount of maximum von Mises stress. This optimized design is what is shown in Figure 5 and Figure 6.

The main reason the optimization process did not aim to minimize max von Mises stress at a fixed vertical displacement is since we wanted to obtain a variety of different MFI designs where some MFI designs are better suited for smaller vertical displacements and others are better suited for larger vertical displacements.

B. Meshing Considerations

To obtain sufficiently accurate FEA-based max von Mises stress results, it is important that a high-quality mesh be implemented as these results are mesh size dependent. Moreover, it is critical to reduce the risk of simulation artifacts (e.g., stress singularities) as these also lead to inaccuracies. To address these challenges, this paper has: 1) taken several steps to avoid stress singularities and 2) evaluated our meshing strategy in order to ensure sufficient mesh granularity to avoid inaccuracies.

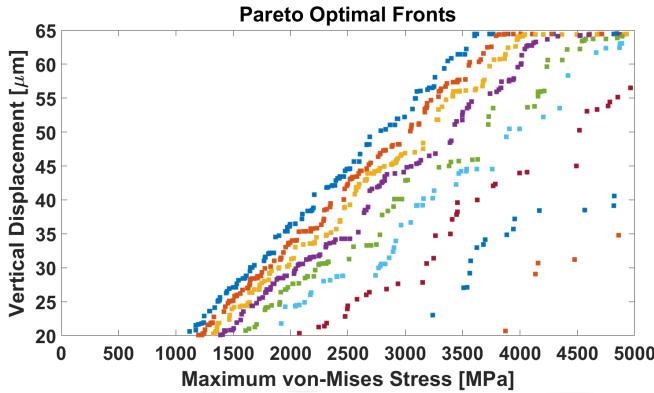


Fig. 8. Pareto front successions resulting from 31 iterations of multi-objective NSGA-II. Final Pareto front is in dark blue (most left).

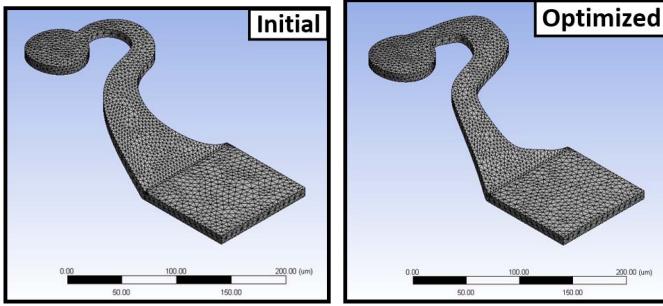


Fig. 9. Mesh for the initial (left) and optimized MFIs (right) as implemented during the optimization process (not adaptive mesh refinement).

To address the matter of stress singularities, extensive efforts were performed to smooth corners and interfaces. Specifically, as aforementioned, spline-based parametrization was implemented, in part, to ensure smoothly-varying structural profiles. In addition, fillets were used extensively to soften sharp edges of the modeled MFI structure.

We also evaluated our meshing profile using the adaptive mesh refinement feature in ANSYS Workbench for both initial and optimized MFIs to test the accuracy of the simulation results. Additionally, we display the original mesh of the initial and optimized MFIs as shown in Figure 9. The adaptive mesh refinement results, shown in Table III, demonstrate that the max von-Mises changes little ($\approx 1\%$ or less) even after a large increase in the number of elements (about an order of magnitude larger) is adaptively added to the mesh.

Since there exists an inherent tradeoff between high fidelity simulations and simulation run time (and therefore overall optimization process time), it is at the discretion of the designer as to how he/she prioritizes these factors. This paper attempted to achieve a sufficiently high-quality mesh for our MFIs while maintaining the average simulation run time to a reasonable limit.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Microfabrication

To provide a more complete analysis of the simulated optimization process, MFIs were microfabricated via a reflowed

TABLE III
ADAPTIVE MESH REFINEMENT FOR THE INITIAL AND OPTIMIZED MFI MESHING

MFI	Refinement Loop	Equivalent Stress (MPa)	Change (%)	Nodes	Elements
Initial	-	1882.5	-	25065	14105
	1	1861.8	-1.11	47551	28804
	2	1873.8	0.64	172127	115276
Optimized	-	1324.2	-	23870	13371
	1	1318.8	-0.41	76769	48432
	2	1319.7	6.8e-2	322868	221308

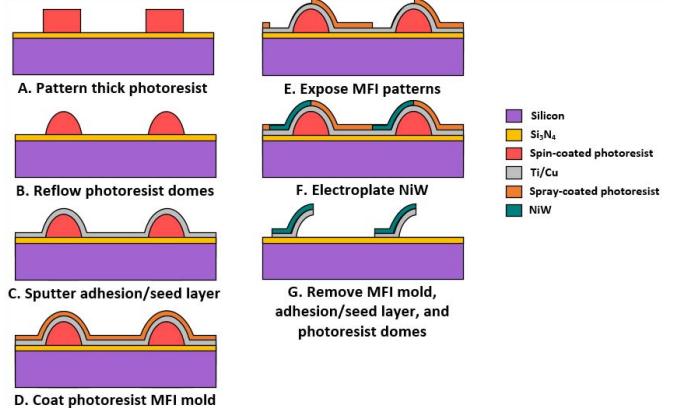


Fig. 10. Fabrication process flow for MFIs.

polymer-dome process [31]–[34], as seen in Figure 10, with the initial and optimized photomask designs. The MFI process flow begins with the patterning of a thick sacrificial spin-coated photoresist layer so that a relatively large stand-off height for the MFIs is attainable. Next, the patterned photoresist is thermally reflowed via exceeding the glass transition temperature (T_g) of the photoresist. A 30 nm thick titanium (Ti) adhesion layer followed by a 300 nm thick Cu seed layer is then sputtered onto the sample. To form the electroplating molds for the MFIs, a photoresist layer is first spray-coated onto the reflowed domes and then patterned. The sample is then placed into an electroplating bath where a NiW alloy is electroplated into the molds. The specifics of the electroplating recipe will be discussed in the next paragraph. Finally, the spray coated photoresist, the Ti adhesion layer and Cu seed layer, and the sacrificial reflowed photoresist dome are removed in sequence, leaving free-standing NiW MFIs. Figure 11 shows an SEM image of several microfabricated optimized MFIs and Figure 12 shows an SEM image of the optimized MFI alongside the initial MFI.

The MFIs were electroplated using the general procedures found in [40] to carry out this process, as we have done in the past [31]–[33]. The electroplated NiW thickness for the MFIs was measured to be approximately 6.9 μm .

Since we desired to plastically deform both initial and optimized MFI samples so that a quantitative comparison between the two designs was possible, the MFIs were fabricated in such a way that plastic deformation of the MFIs was observable for a given indentation depth. To this end, the NiW yield strength was deliberately decreased via using a lower tungsten

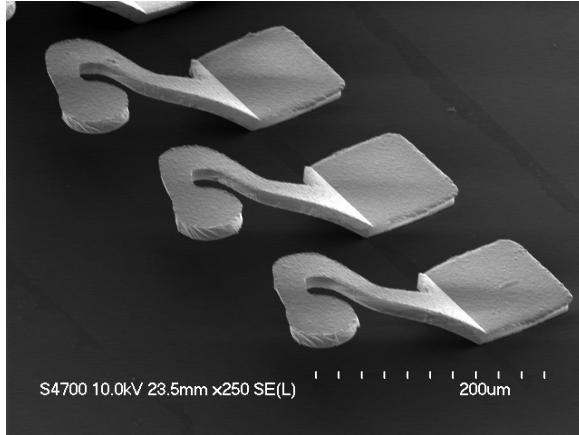


Fig. 11. SEM image of optimized MFIs.

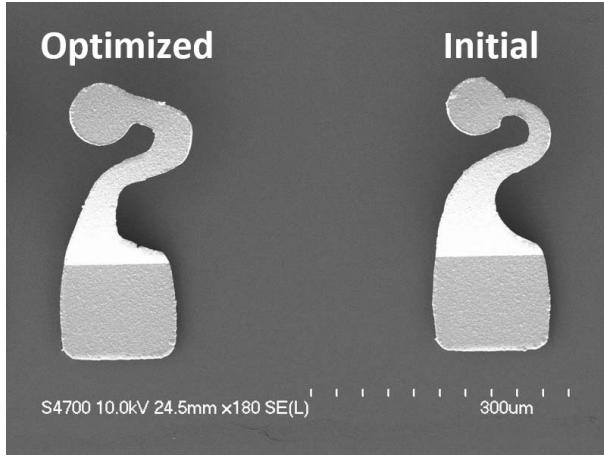


Fig. 12. SEM image of the optimized MFI (left) and initial, non-optimized MFI (right).

concentration in the plating solution. A higher tungsten concentration (i.e., 20 g/l sodium tungstate dihydrate [40]) added to the Ni sulfamate plating solution contributes to a higher yield strength such that only elastic deformation may occur over a full indentation (i.e., indented up to the point where the MFI tip touches the substrate).

B. Measurements and Data Analysis

Figure 13 illustrates a flowchart of the measurement extraction process followed in this paper. After electroplating and fabricating our structures, we indented our MFIs using a Hysitron Triboindenter with a Cono-Spherical probe to obtain load (and unload) vs. displacement data. From these measurements, we sought to determine two data points for each indented MFI: 1) the amount of vertical plastic deformation, as seen in Figure 14, and 2) the mechanical compliance. Figure 15 shows the raw load vs. displacement data of closely located initial and optimized MFIs, both indented to a depth of 45 μ m.

To analyze this data more accurately, a best fit piecewise linear curve (or first-order spline) was implemented using MATLAB built-in functions on the loading and unloading

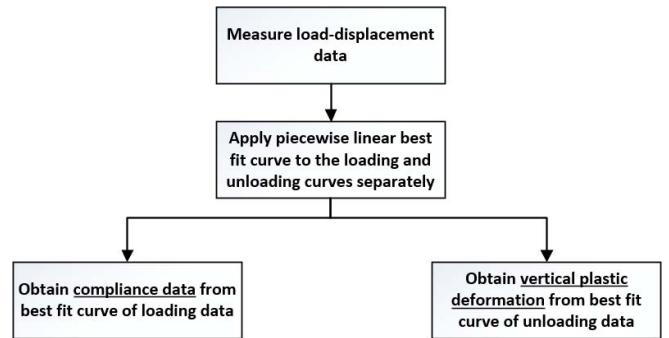


Fig. 13. Flowchart illustration of the experimental data extraction process.

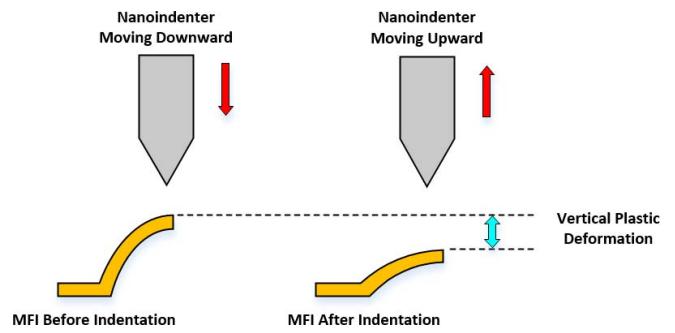


Fig. 14. MFI side-view illustration shown before indentation occurs and after indentation occurs. This single indentation induces a certain vertical plastic deformation (if yield strength is exceeded).

TABLE IV
COMPLIANCE FOR INITIAL AND OPTIMIZED MFI PAIRS

Sample	Initial MFI Compliance (mm/N)	Optimized MFI Compliance (mm/N)
1	11.17	12.10
2	10.57	12.42
3	11.31	11.69
4	11.13	14.09
5	11.19	11.49
6	10.93	12.75
7	10.20	11.23
Average	10.93	12.25

portions of the raw data as seen in Figure 15. The interior knots of the piecewise linear curve were positioned such that the overall curve was a best fit to the raw data; specifically, the sum of squares due to error (SSE) of the best fit curve with respect to the data was minimized for a given number of interior knots. The best fit curves seen in Figure 16 were applied to the unloading portions of the raw data seen in Figure 15. As seen in Figure 16, the vertical plastic deformation is extracted from the best fit curve.

Table IV shows the experimentally-obtained compliance measurements. Recall that the fabricated MFI thickness was measured to be approximately 6.9 μ m as opposed to the simulated MFI thickness of 9 μ m. Therefore, as expected,

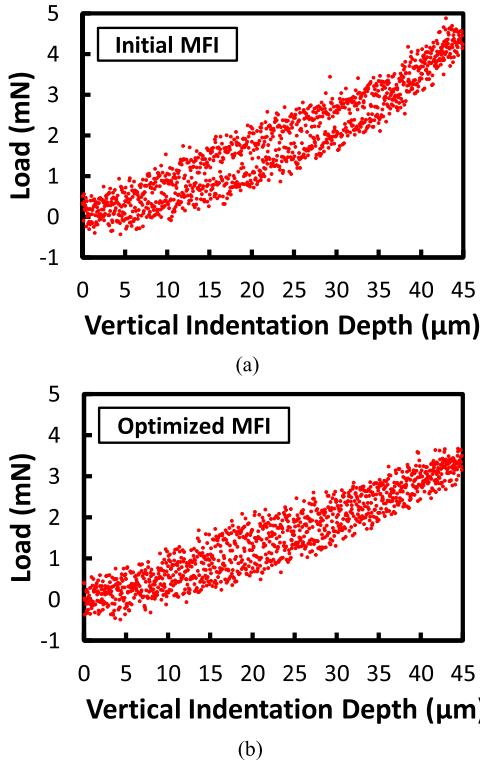


Fig. 15. Raw “load vs. displacement” data for an MFI pair, (a) initial and (b) optimized, indented to a vertical depth of 45 μm .

TABLE V
EXPERIMENTAL AND SIMULATED COMPLIANCE FOR INITIAL
AND OPTIMIZED 6.9 μm THICK MFI PAIRS

Data Type	Initial MFI Compliance (mm/N)	Optimized MFI Compliance (mm/N)
Experimental (Avg.)	10.93	12.25
Simulation	9.69	11.10

the measured compliance is higher than the simulated compliance.

To more specifically compare against the aforementioned experimental compliance data, 6.9 μm thick MFIs were simulated to obtain compliance. As seen in Table V, we obtain a simulated compliance of 9.69 mm/N and 11.10 mm/N for the initial MFI design and the optimized MFI design, respectively. The main source of discrepancy between the experimental data and the simulation data may potentially derive from a difference in the Young’s modulus used in the simulation (i.e., 180 GPa [40], [41]) and the actual Young’s modulus of the microfabricated MFIs. Differences in geometry between simulated and optimized MFIs may also play a role.

In an effort to obtain vertical plastic deformation measurements, this same implementation of a best fit piecewise linear curve was performed on the remaining additional raw unloading data and is recorded in Figure 17. Comparisons in Figure 17 between optimized MFIs and initial MFIs are done for different MFI samples or pairs. In this paper, MFI pairs are defined as an initial MFI and an optimized MFI

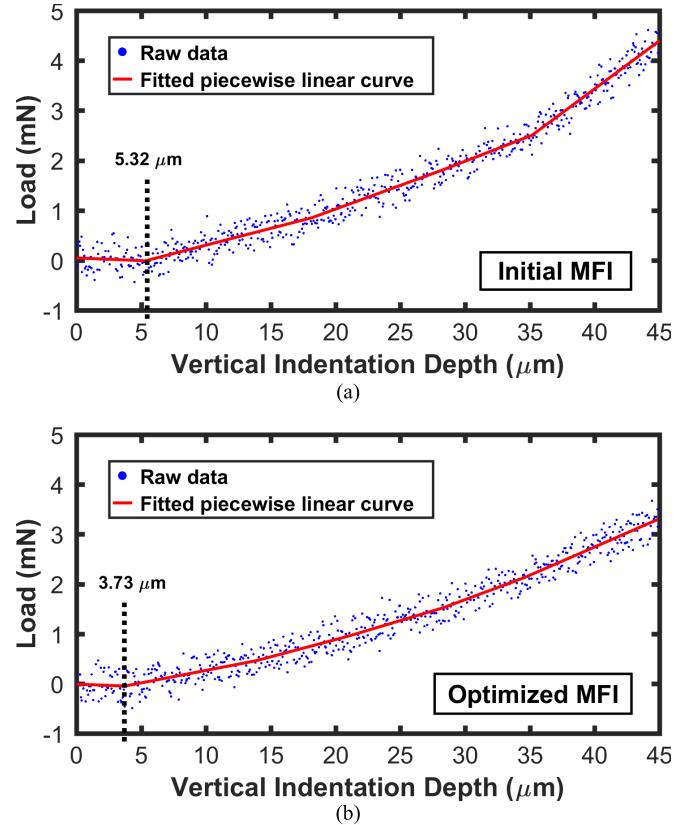


Fig. 16. Unloading portion of the experimental load-displacement data with a best fit piecewise linear curve. Data for (a) initial MFI and (b) optimized MFI both indented to a depth of 45 μm is shown.

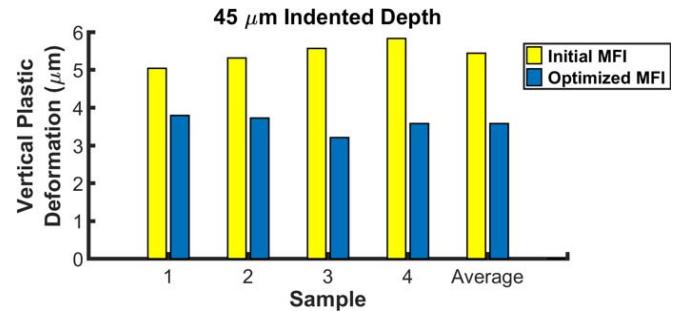


Fig. 17. Vertical plastic deformation of optimized and initial MFI samples for MFIs indented to a depth of 45 μm .

that are physically near each other on the Si wafer (on the same polymer dome for example) so that geometric parameters such as height and thickness are as similar as possible for the two structures. As seen in Figure 17, the average vertical plastic deformation for the initial MFI and the optimized MFI indented to a depth of 45 μm is 5.44 μm and 3.58 μm , respectively, a 34.2% average decrease in vertical plastic deformation for the optimized MFI.

To reiterate, the observed plastic deformation of the MFIs was intentionally desired so that a quantitative comparison between initial and optimized designs was possible. Typically, we wish to avoid plastic deformation. As aforementioned, increasing the yield strength of the electroplated NiW is one

means by which such plastic deformation is avoided. This elastic-only behavior (up to 65 μm) has been reported with our MFIs in the past [33].

V. CONCLUSION

This paper introduced a generalized optimization methodology for MEMS-type flexible interconnects using a multi-objective, non-dominated sorting genetic algorithm-II (NSGA-II) to minimize maximum von Mises stress and maximize vertical displacement while maintaining a compliance within a targeted range. Relative to the initial NiW MFI design, the simulated results for the optimized MFI demonstrate an increase of 29.7% in vertical displacement before the MFI's max von Mises stress exceeded its yield strength. After microfabrication of the NiW MFIs, indentations were performed on these MFIs and load vs. displacement data were collected. To more accurately analyze and interpret this data, a best-fit piecewise linear curve was implemented from which compliance and vertical plastic deformation was extracted. The optimized microfabricated MFI demonstrated a 34.2% decrease in vertical plastic deformation relative to the initial MFI for a 45 μm indentation depth. In both simulation and experimental scenarios, the optimized MFI demonstrated less stress/plastic deformation relative to the initial MFIs for the same given indented depth, as intended.

ACKNOWLEDGMENT

This work was performed in part at the Georgia Tech Institute for Electronics and Nanotechnology, a member of the National Nanotechnology Coordinated Infrastructure.

REFERENCES

- [1] M. S. Bakir, B. Dang, R. Emery, G. Vandentop, P. A. Kohl, and J. D. Meindl, "Sea of leads compliant I/O interconnect process integration for the ultimate enabling of chips with low- K interlayer dielectrics," *IEEE Trans. Adv. Packag.*, vol. 28, no. 3, pp. 488–494, Aug. 2005.
- [2] M. S. Bakir *et al.*, "Sea of Leads (SoL) ultrahigh density wafer-level chip input/output interconnections for gigascale integration (GSI)," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2039–2048, Oct. 2003.
- [3] B. Dang, M. S. Bakir, C. S. Patel, H. D. Thacker, and J. D. Meindl, "Sea-of-leads MEMS I/O interconnects for low- K IC packaging," *J. Microelectromech. Syst.*, vol. 15, no. 3, pp. 523–530, Jun. 2006.
- [4] K. Kacker, G. C. Lo, and S. K. Sitaraman, "Low- K dielectric compatible wafer-level compliant chip-to-substrate interconnects," *IEEE Trans. Adv. Packag.*, vol. 31, no. 1, pp. 22–32, Feb. 2008.
- [5] K. Kacker and S. K. Sitaraman, "Electrical/mechanical modeling, reliability assessment, and fabrication of flexconnects: A MEMS-based compliant chip-to-substrate interconnect," *J. Microelectromech. Syst.*, vol. 18, no. 2, pp. 322–331, Apr. 2009.
- [6] Q. Zhu, L. Ma, and S. K. Sitaraman, " β -Helix: A lithography-based compliant off-chip interconnect," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 26, no. 3, pp. 582–590, Sep. 2003.
- [7] P. Xu, A. H. Pfeiffenberger, C. D. Ellis, and M. C. Hamilton, "Fabrication and characterization of double helix structures for compliant and reworkable electrical interconnects," *J. Microelectromech. Syst.*, vol. 23, no. 5, pp. 1219–1227, Oct. 2014.
- [8] S. Muthukumar *et al.*, "High-density compliant die-package interconnects," in *Proc. 56th Electron. Compon. Technol. Conf.*, May/Jun. 2006, pp. 1233–1238.
- [9] I. Shubin *et al.*, "Novel packaging with rematable spring interconnect chips for MCM," in *Proc. 59th Electron. Compon. Technol. Conf.*, May 2009, pp. 1053–1058.
- [10] L. Ma, Q. Zhu, T. Hantschel, D. K. Fork, and S. K. Sitaraman, "J-springs—Innovative compliant interconnects for next-generation packaging," in *Proc. 52nd Electron. Compon. Technol. Conf.*, May 2002, pp. 1359–1365.
- [11] R. B. Marcus, "A new coiled microspring contact technology," in *Proc. 51st Electron. Compon. Technol. Conf.*, May/Jun. 2001, pp. 1227–1232.
- [12] P. K. Jo, M. Zia, J. L. Gonzalez, H. Oh, and M. S. Bakir, "Design, fabrication, and characterization of dense compressible microinterconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 7, pp. 1003–1010, Jul. 2017.
- [13] J. Li *et al.*, "An electromechanical model and simulation for test process of the wafer probe," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 1284–1291, Feb. 2017.
- [14] J. Li, W. Tian, H. Liao, C. Zhou, X. Liu, and W. Zhu, "The mathematical model and novel final test system for wafer-level packaging," *IEEE Trans. Ind. Informat.*, vol. 13, no. 4, pp. 1817–1824, Aug. 2017.
- [15] W. Chen, R. Okereke, and S. K. Sitaraman, "Compliance analysis of multi-path fan-shaped interconnects," *Microelectron. Rel.*, vol. 53, no. 7, pp. 964–974, Jul. 2013.
- [16] W. Chen and S. K. Sitaraman, "Area-array of 3-arc-fan compliant interconnects as effective drop-impact isolator for microsystems," *J. Microelectromech. Syst.*, vol. 25, no. 2, pp. 337–346, Apr. 2016.
- [17] W. Chen, Y. Song, J. Liang, and S. K. Sitaraman, "Fabrication of second-level tridelta interconnects using negative dry-film photoresist," in *Proc. ASME Int. Mech. Eng. Congr. Expo.*, Montreal, QC, Canada, vol. 10, Nov. 2014, pp. V010T13A041-1–V010T13A041-6, Paper IMECE2014-40154, doi: [10.1115/IMECE2014-40154](https://doi.org/10.1115/IMECE2014-40154).
- [18] W. Chen, A. Bhat, and S. K. Sitaraman, "Impact isolation through the use of compliant interconnects for microelectronic packages," *J. Electron. Packag.*, vol. 137, no. 4, p. 041005, Oct. 2015.
- [19] W. Chen, "Design, fabrication, and reliability study of second-level compliant microelectronic interconnects," Ph.D. dissertation, Georgia Inst. Technol., Atlanta, GA, USA, Jul. 2015. [Online]. Available: <http://hdl.handle.net/1853/55550>
- [20] W. Chen, A. Bhat, and S. K. Sitaraman, "Use of compliant interconnects for drop impact isolation," in *Proc. IEEE 63rd Electron. Compon. Technol. Conf.*, May 2013, pp. 835–839.
- [21] R. Labie, W. Ruythooren, K. Baert, E. Beyne, and B. Swinnen, "Resistance to electromigration of purely intermetallic micro-bump interconnections for 3D-device stacking," in *Proc. Int. Interconnect Technol. Conf.*, Jun. 2008, pp. 19–21.
- [22] J. Li, L. Han, J. Duan, and J. Zhong, "Interface mechanism of ultrasonic flip chip bonding," *Appl. Phys. Lett.*, vol. 90, no. 24, p. 242902, 2007.
- [23] R. Chaware, K. Nagarajan, and S. Ramalingam, "Assembly and reliability challenges in 3D integration of 28nm FPGA die on a large high density 65nm passive interposer," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf.*, May/Jun. 2012, pp. 279–283.
- [24] K. M. Chen, D. S. Jiang, N. H. Kao, and J. Y. Lai, "Effects of underfill materials on the reliability of low- K flip-chip packaging," *Microelectron. Rel.*, vol. 46, no. 1, pp. 155–163, Jan. 2006.
- [25] Z. Kornain, N. Amin, A. Y. Cheah, and A. Jalar, "An approach on underfill material selection for the low- K flip chip plastic ball grid array (FCPBGA)," in *Proc. 33rd IEEE/CPMT Int. Electron. Manuf. Technol. Symp. (IEMT)*, Nov. 2008, pp. 1–6.
- [26] P.-H. Tsao, C. Huang, M.-J. Lii, B. Su, and N.-S. Tsai, "Underfill characterization for low- K dielectric / Cu interconnect IC flip-chip package reliability," in *Proc. 54th Electron. Compon. Technol. Conf.*, vol. 1, Jun. 2004, pp. 767–769.
- [27] M.-C. Paquet, M. Gaynes, E. Duchesne, D. Questad, L. Belanger, and M. Sylvestre, "Underfill selection strategy for Pb-free, low- K and fine pitch organic flip chip applications," in *Proc. 56th Electron. Compon. Technol. Conf.*, May/Jun. 2006, pp. 1595–1603.
- [28] Z. Zhang and C. P. Wong, "Recent advances in flip-chip underfill: Materials, process, and reliability," *IEEE Trans. Adv. Packag.*, vol. 27, no. 3, pp. 515–524, Aug. 2004.
- [29] Z. Feng, W. Zhang, B. Su, K. C. Gupta, and Y. C. Lee, "RF and mechanical characterization of flip-chip interconnects in CPW circuits with underfill," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 12, pp. 2269–2275, Dec. 1998.
- [30] H. Kusamitsu, Y. Morishita, K. Maruhasi, M. Ito, and K. Ohata, "The flip-chip bump interconnection for millimeter-wave GaAs MMIC," *IEEE Trans. Electron. Packag. Manuf.*, vol. 22, no. 1, pp. 23–28, Jan. 1999.
- [31] C. Zhang, H. S. Yang, H. D. Thacker, I. Shubin, J. E. Cunningham, and M. S. Bakir, "Mechanically flexible interconnects with contact tip for rematable heterogeneous system integration," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 11, pp. 1587–1594, Oct. 2016.
- [32] C. Zhang, H. S. Yang, and M. S. Bakir, "Mechanically flexible interconnects (MFIs) with highly scalable pitch," *J. Micromech. Microeng.*, vol. 24, no. 5, p. 055024, 2014.

- [33] C. Zhang, H. S. Yang, and M. S. Bakir, "Highly elastic gold passivated mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1632–1639, Oct. 2013.
- [34] H. S. Yang and M. S. Bakir, "Design, fabrication, and characterization of freestanding mechanically flexible interconnects using curved sacrificial layer," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 4, pp. 561–568, Apr. 2012.
- [35] E. B. Liao *et al.*, "A MEMS-based compliant interconnect for ultra-fine-pitch wafer level packaging," in *Proc. 56th Electron. Compon. Technol. Conf.*, May/Jun. 2006, pp. 1246–1250.
- [36] E. M. Chow, D. K. Fork, C. L. Chua, K. Van Schuylenbergh, and T. Hantschel, "Wafer-level packaging with soldered stress-engineered micro-springs," *IEEE Trans. Adv. Packag.*, vol. 32, no. 2, pp. 372–378, May 2009.
- [37] W. Chen and S. K. Sitaraman, "Response surface and multiobjective optimization methodology for the design of compliant interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 11, pp. 1769–1777, Nov. 2014.
- [38] Q. Zhu, L. Ma, and S. K. Sitaraman, "Design optimization of one-turn helix: A novel compliant off-chip interconnect," *IEEE Trans. Adv. Packag.*, vol. 26, no. 2, pp. 106–112, May 2003.
- [39] J. Sacks, W. J. Welch, T. J. Mitchell, and H. P. Wynn, "Design and analysis of computer experiments," *Statist. Sci.*, vol. 4, no. 4, pp. 409–423, Nov. 1989.
- [40] E. Slavcheva, W. Mokwa, and U. Schnakenberg, "Electrodeposition and properties of NiW films for MEMS application," *Electrochim. Acta*, vol. 50, no. 28, pp. 5573–5580, Sep. 2005.
- [41] J. Luo, A. J. Flewitt, S. M. Spearing, N. A. Fleck, and W. I. Milne, "Young's modulus of electroplated Ni thin film for MEMS applications," *Mater. Lett.*, vol. 58, nos. 17–18, pp. 2306–2309, 2004.



Joe L. Gonzalez (S'15) received the B.S. (Hons.) degree and the M.S. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2012 and 2014, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interests include improving the mechanical and electrical characteristics of MEMS-type flexible interconnects for 2.5D/3D IC systems in addition to developing biosensor modules.



Paul K. Jo (S'15) received the B.S. (Hons.) degree and the M.S. degree in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2009 and 2011, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with the Georgia Institute of Technology, Atlanta, GA, USA.

His current research interests include 2.5D/3D heterogeneous integration and biosensor application using novel micro-fabricated flexible interconnect technologies.



Reza Abbaspour (S'10) received the master's degrees in telecommunication engineering and integrated photonics from the University of Vaasa, Finland and the Georgia Institute of Technology (Georgia Tech), USA, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with a minor in material science with Georgia Tech. Prior to that, he was a Research and Development Engineer in Finland.



Muhammed S. Bakir (SM'12) received the B.E.E. degree from Auburn University, Auburn, AL, USA, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech) in 2000 and 2003, respectively.

He is currently a Professor with the School of Electrical and Computer Engineering, Georgia Tech. His areas of interest include 3-D electronic system integration, advanced cooling and power delivery for 3D systems, biosensors and their integration with CMOS circuitry, and nanofabrication technology. He was a recipient of the 2013 Intel Early Career Faculty Honor Award, the 2012 DARPA Young Faculty Award, and the 2011 IEEE CPMT Society Outstanding Young Engineer Award. He and his research group have received over 20 conference and student paper awards, including six from the IEEE Electronic Components and Technology Conference, four from the IEEE International Interconnect Technology Conference, and one from the IEEE Custom Integrated Circuits Conference. His group received the 2014 Best Paper of the IEEE TRANSACTIONS ON COMPONENTS PACKAGING AND MANUFACTURING TECHNOLOGY in the area of advanced packaging. He was an Invited Participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium. In 2015, he was elected by the IEEE CPMT Society to serve as a Distinguished Lecturer.

Dr. Bakir serves on the Editorial Board of the IEEE TRANSACTIONS ON ELECTRON DEVICES and the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY.